Electromigration and IR Voltage Drop Reduction Technique on DDR Memory Block Using Power Grid Augmentation

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#### **Abstract—As technology scales down to nanometres it severely affects the IR (Voltage) drop. Although checking this problem in the earlier stages can speed up the analysis, not many tools are available to fix this. Recently Redhawk has included a new feature to fix the electromigration (EM) and IR voltage drop and achieve signoff. It significantly reduces the manual effort required to minimize the electromigration and IR (EMIR). In this paper, a double data rate (DDR) memory block is implemented using 14 nm technology, the EM and IR voltage drop are analysed. The proposed design has reduced the IR voltage drop values to less than 2% of the VDD value (0.99 V), and concerning EM variation could converge to around 83%. Typically, the value of the EM violations should be less than 100%. Hotspot reduction has been done by adding the metal strips. Thus, it can be concluded that by adding metal strips, and by providing a stronger power delivery network (PDN), we can mitigate the hotspots and therefore reduce the IR voltage drop and EM violations. The worst violated path in the static run before clearing violations is in the Metal (M1) layer has a value of 28.50 mV, and EM violating path is 192%. The total power consumption is found to be 4.11 W before clearing the static EMIR run violations. The worst violating path for the static run after clearing violations is in the M1 layer has a value of 5.60 mV. The total power consumption is measured to be 1.4 W for the static run after clearing violations and, EM violating path is put down to 83%. After using power grid augmentation (PGA), the total power consumption is reduced to 1.29 W. Therefore, there is an IR voltage drop of 28.5mV before PGA and 5.6mV after PGA. From the existing methodology (double row optimization) we can see an IR voltage drop of 29mV as the worst instance drop.**

Keywords— EMIR reduction, PG augmentation, Redhawk, EMIR signoff, ICC2 Fusion, DDR memory

# Introduction

Memories are categorized as volatile and non-volatile. Volatile memory consists of random-access memory (RAM), dynamic random-access memory (DRAM), synchronous dynamic random-access memory (SDRAM) and DDR SDRAM. Primary memory that reacts quickly is required for all battery-operated devices. Static RAM is frequently utilized as cache memory and main memory in many applications due to its high speed and performance. But read destruction is a significant problem in SRAM cells [1]. The cache memory is made up of several SRAM cells, because they are highly durable, run at low power, and volatile. They continue to be the most significant in all memory technologies. As the name implies, an SRAM cell provides access to read stored data and rewrite data as needed [2]. Whereas DDR has the capability of transferring the data in both positive and negative edges of the clock pulse [3]. While scaling down to lower nanometer technology, the back end of line (BEOL) resistance increases with a decrease in the layers thickness. The increase in resistance impacts delay, thereby requiring more buffers to overcome this delay [4]. An increase in propagation delay is observed when the threshold voltage of MOSFET is more than the supply voltage.[5]

The Integrated Circuit Compiler (ICC2) Fusion tool has the capability to power grid (PG) augment and fix EMIR. IR voltage drop typically consists of both resistance and an inductance element. By optimizing the PG, the IR voltage drop can be minimized. The inductive form of IR voltage drop can be reduced by varying the rate of change of current and the overall inductance of the design [6].

Static IR voltage drop is dependent on the resistance and capacitance of the PG which connects the power supply to the standard cells. Gate – Channel leakage current plays an important role in the static IR drop. The design average current depends on the time period of the metal stripes added in the design.

In this paper, power EM static EMIR run is performed with a voltage value of 0.99 V at a temperature of 110°C. The process used for the EMIR run is typical (tt). To reduce the designer’s manual efforts, the PGA technique is used. Using this technique, metal strips are added at the high EM and IR violating regions. Due to this, the high current at those regions is diverted to these strips. As the current density is mitigated, the EM violations drop down in those regions. Mitigation of EM violations were performed traditionally following the Black’s EM equation that is by increasing the width of the metal layer where the EM violation was found. Other traditional way is to increase the connectivity of the vias, so that we don’t have EM violations in the design. As we reduce EM violations indirectly IR voltage drop reduces.

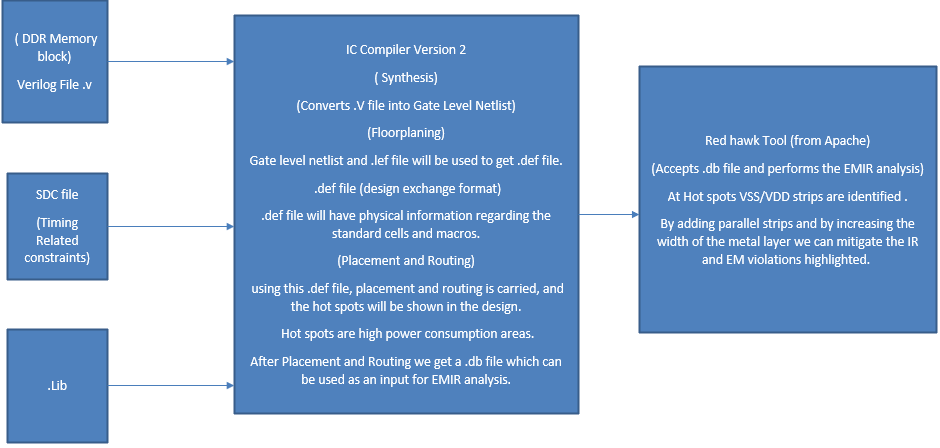
In this paper, Section II represents the flow of the analysis used from RTL design to routing and the Redhawk flow. Section III gives a brief description about EM and IR voltage drop issues and a few standard ways to mitigate them. Section IV explains about the new PGA approach and its effect on EM and IR voltage drop. Section V contains the results and discussion which are the run results after and before clearing the EM violations and IR voltage drop using & without using PGA. Highlighted EM and IR maps of the DDR memory blocks can be seen in the Section V with the hotspots. Section VI concludes with the final remarks and the future scope.

# Flow of analysis

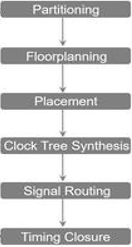
## RTL - Routing flow

The EMIR flow involves RTL – Routing Steps. For the EMIR analysis, the Routed db is used after performing the synthesis, floor planning, placement, and routing steps. The Design Compiler needs: 1) V file (Netlist) 2) Lib (library) 3) SDC (Synopsys Design Constraints) files to run the synthesis. After running the synthesis, a gate level Verilog netlist file is generated as the output. The output file is dumped along with the technology file(.tech) to provide the lef file (library exchange format), which contains the physical information to perform floor planning. The Routed db is generated after the routing stage, which is used to perform the EMIR analysis. The Synthesis to EMIR flow is illustrated in Fig. 1. The ICC2 complier is used for floor planning, placement, clock tree synthesis and routing. The basic flow is illustrated in Fig. 2.

EMIR analysis is performed using the Apache Redhawk tool. In this tool, the high voltage regions in the design are highlighted and the EM problems can also be investigated. Power rings are added in higher-level routing layers to perform signal routing in lower layers. The trade-off between IR voltage drop and EM routing resources is as follows 1) wider the power lines lesser the static, dynamic and EM. 2) lesser the signal routing resources higher is the congestion. The total number of strips and interval distance is dependent on the core power consumption. As power consumption (static and dynamic) increases, the distance between power and ground straps interval increases and this reduces the overall IR voltage drop, thereby improving the performance.



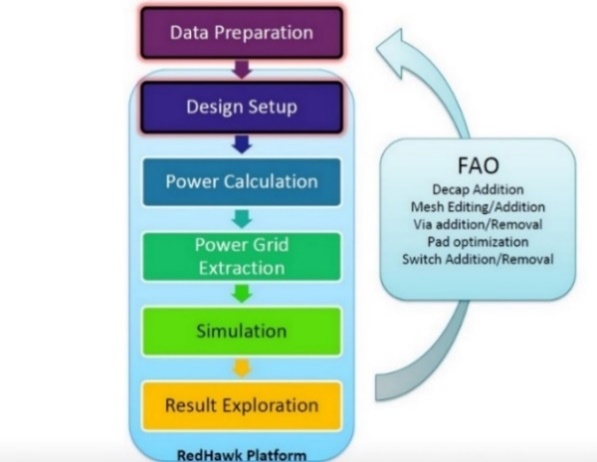
**Fig. 1. The Basic Steps from Synthesis to EMIR**



**Fig. 2. Physical Design Flow**

## Redhawk Methodology and Flow

Redhawk analysis flow initially consists of the data preparation step and the design setup step. After the design setup, we have the power calculation and resistance extraction steps followed by simulation and result files extraction. The same is represented in Fig. 3.



**Fig. 3. Redhawk Flow**

The static run mainly depends on the toggle rate present in the Global System Requirements (GSR) file:

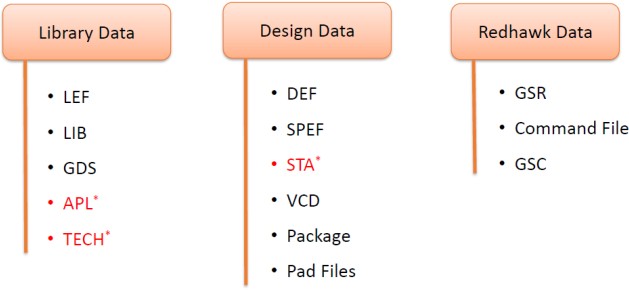
1)Toggle is 0 to 1 or 1 to 0 transition.

2)Toggle rate = (no. of transitions) / (no. of cycles)

3)Toggle rate of CLK= 2 4 and Toggle rate of SIGNAL=0.3

GSR keyword uses TOGGLE\_RATE 0.3 2

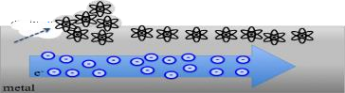
The toggle rate can be varied and checked for EM violations by adjusting these variables in the GSR file. For the Redhawk EMIR run, the following inputs highlighted in red along with GSR file are needed, as shown in the Fig. 4.



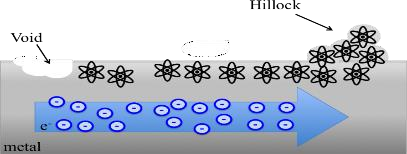
**Fig. 4. Inputs Required for Redhawk EMIR Run**

# Electromigration and IR Voltage Drop

Electromigration is an increasing concern in on-chip wires and vias in future technologies. EM failures may occur when current flows through a wire over a long period of time in the design, and the current density is high enough to cause a physical migration of atoms in the wire. High temperatures and higher current densities (which increase the dragging force) increase metal atoms’ likelihood to move. Therefore, the drift of metal atoms, causes the voids and hillocks due to which EM occurs in the circuit design. This is illustrated in the Fig 5.1 and Fig. 5.2 respectively. To check the EM reliability, all the existing methods use the current density of individual wires as the constraint, which is mainly based on the Black’s EM model [7].

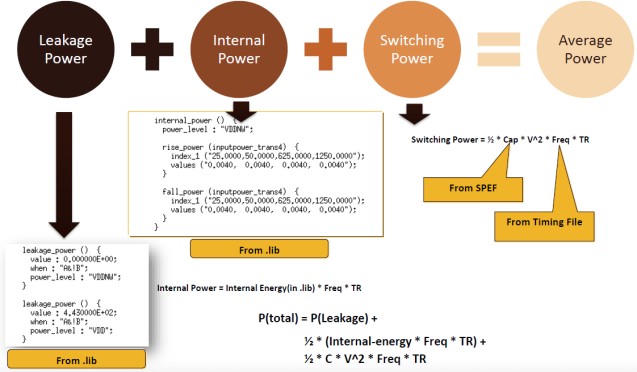


**Fig. 5.1. The Drift of Metal Atoms with The Flow of Electrons**



**Fig. 5.2. Voids and Hillocks**

Voltage drop is the decrease of electric potential along the path of current flow. Voltage drops across the source resistance, conductors, contacts, and connectors gives rise to unwanted power dissipation. IR voltage drop and EM are two major problems while the scaling of technology goes below 45 nm. As technology scales down the leakage power in the CMOS circuit increases [8][9]. The different power calculations are shown in Fig. 6.



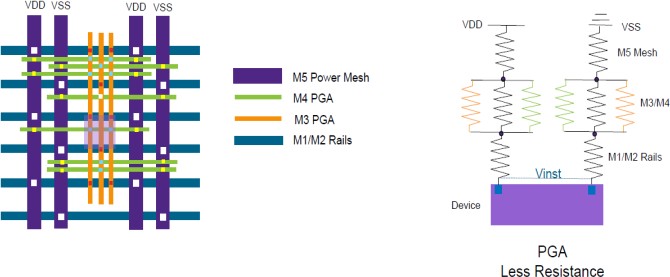
**Fig. 6. Power Calculation**

Hold violations are caused due to the IR voltage drop impact on the clock networks, while IR voltage drop on data path signal net causes setup violations. Therefore, the standard cells are separated from macros to ensure lesser effort on any bump. In the proposed design, Redhawk Apache tool is used for the Standalone run of Static EMIR which mitigates the IR voltage drop to go below two percent of the VDD (0.99 V). EM violations are minimized (almost Nil) after performing a couple of fixes with respect to the decoupling of capacitors and vias addition.

# Power Grid Augmentation

After EMIR analysis, the hotspots are fixed. ICC2 fusion adds extra power and ground straps to reduce IR voltage drop and current density, which in turn reduces the EM violations. The Redhawk tool does the power strap insertion based on hotspots while keeping design rule check (DRC) in view. It also does PG Augmentation with minimum impact to timing. Redhawk can be refined to augment straps efficiently by using customized parameter file. This customized parameter file can control certain layer-specific widths, spacings and settings in the proposed design. By using this efficiently, more metal shapes were inserted in the design. RC (delay) is re-estimated for the new PG. Filling these shapes in different hotspot regions has thus improved IR and removed EM violations [10].

The Redhawk tool identifies the hotspots with excessive voltage drop in the PG. The PG is augmented by adding local conductors at the hotspots. These local conductors provide additional electrical paths for the hotspots. This in turn reduces the voltage drops at the hotspots as shown in Fig. 7.



**Fig. 7. Power Grid Augmentation**

Excessive voltage drops across metal shapes can cause the final delivered voltage to be too low. PGA is one approach to address these excessive voltage drops. In one of the approaches to PGA, metal fill is used to augment the PG. Metal fills are metal shapes that are added to the integrated circuit design to physically fill out the design. Metal fill serves a structural purpose; hence a metal fill is typically not connected to any of the electrical nets in the integrated circuit. The trailing metal fills are found to be “floating” in the design. These floating fill shapes are then used to augment the PG by dropping vias at appropriate intersections between the fill shapes and the PG [11].

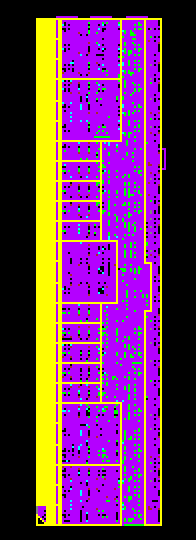
The PGA is timing dependent. The effect on timing is used to determine the number of local conductors that needs to be added. In one of the approaches, the flow protects the clock and timing critical nets by not placing any additional conductors near them, thus reducing the timing impact. When timing effects cannot be avoided, local conductors that have a maximum impact on reducing resistance are selected, while having a minimum impact on timing [12][13].

# Results and Discussion

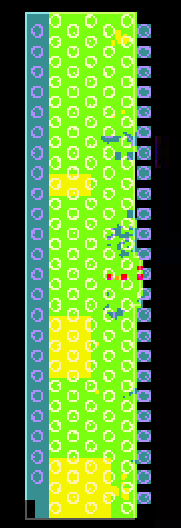
PGA has enhanced the capabilities of the designer to automate the fixes by adding parallel resistors wherever required by identifying the hotspots in the design. This technique has become handy in recent times by reducing the manpower. The proposed DDR cell memory block has been implemented using 14 nm technology and EMIR analysis is performed on it, as shown in Fig .8. This block involves the use of standard cell logics with the filler and physical cells.

Clock Information and Sinks: There are six generated clocks and twelve propagated master clocks in the design with the following time periods as specified in the Table I.

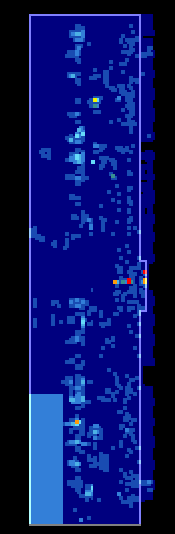
Static EMIR Run Results (Before Clearing the EM Violations): After the Static EMIR run has been performed, 56 EM violations and a worst IR voltage drop of 28 mV have been encountered. The power map and hotspots are highlighted in the Fig. 9 and 10.



**Fig. 8. 14 nm DDR Memory Block**



**Fig. 9. IR Map of DDR**



**Fig. 10. EM Map of DDR Block**

1. Clock Specifications

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Name** | **Source** | **Generated** | **Propagated**  **clk** | **Period(ns)** | **Waveform** |
| APBCLK | {APBCLK} | FALSE | TRUE | 10 | {0 5} |
| APBCLK\_Vir | {} | TRUE | FALSE | 10 | {0 5} |
| BypassPclk | {BypassPclk} | FALSE | TRUE | 0.31 | {0 0.15625 |
| DfiClk | {DfiClk} | FALSE | TRUE | 1.25 | {0 0.625} |
| DfiClk\_Vir | {} | TRUE | FALSE | 1.25 | {0 0.625} |

The worst Static IR voltage drop paths in the design are found in the M1 layer with 14.80 mV for VDD and 17.50 mV for VSS as shown in the Table II.

|  |  |  |  |
| --- | --- | --- | --- |
| **Type** | **Value(mV)** | **Net** | **Ideal Voltage (V)** |
| WIRE | 14.80 | VDD | 0.99 |
| WIRE | 17.50 | VSS | 0 |
| INST | 28.50 | VDD | 0.99 |

1. Worst Static IR drop

The top EM worst paths are found in the wire and via as shown in the Table III.

1. Worst Static EM

|  |  |  |  |
| --- | --- | --- | --- |
| **Type** | **Value** | **Net** | **EM limit (mA)** |
| WIRE | 190.40% | VSS | 35.54 |
| VIA | 56.29% | VDD | 2.54 |

The total power calculations for the static run including the leakage power for different cells are given in the Table IV. Here different powers like leakage power, internal power, switching power and the total power of the design cells are calculated.

1. Power Calculation Before Clearing EM Violations

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **cell\_type** | **Total Power(W)** | **Leakage Power(W)** | **Internal Power(W)** | **Switching Power(W)** |
| combinational | 2.20 | 0.015 | 0.922 | 1.26 |
| latch and FF | 0.583 | 0.0022 | 0.485 | 0.096 |
| memory | 0.136 | 0.00406 | 0.130 | 0.00159 |
| I/O | 0.000 | 0.000 | 0.000 | 0.000 |
| misc\_seq | 1.20 | 0.00022 | 1.18 | 0.0132 |
| decap | 0.000663 | 0.00066 | 0.000 | 0.000 |
| Total | 4.12 | 0.022 | 2.72 | 1.37 |

Static EMIR Run Results (After Clearing the EM Violations): At one percent drop of VDD (that is 0.0099), no violating paths were found in the Static EMIR run. The worst IR voltage drop in the design after clearing the EM violations are shown in Table V.

1. Worst Static IR Drop

|  |  |  |  |
| --- | --- | --- | --- |
| **Type** | **Value (mV)** | **Net** | **Ideal Voltage (V)** |
| WIRE | 3.40 | VDD | 0.99 |
| WIRE | 3.30 | VSS | 0 |
| INST | 5.60 | VDD | 0.99 |

Top EM highlighted spots after clearing the EM violations are shown in Table VI.

1. Worst Static EM Hotspots

|  |  |  |  |
| --- | --- | --- | --- |
| **Type** | **Value** | **Net** | **EM limit (mA)** |
| WIRE | 83.58% | VSS | 27.88 |
| VIA | 15.11% | VSS | 24.30 |

The power for static run after clearing violations is tabulated in Table VII.

1. Power Calculations After Clearing EM Violations

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cell type** | **Total Power(W)** | **Leakage Power(W)** | **Internal Power(W)** | **Switching Power(W)** |
| Combinational | 0.199 | 0.0145 | 0.112 | 0.0734 |
| Latch and FF | 0.128 | 0.0022 | 0.125 | 0.00034 |
| Memory | 0.00513 | 0.00406 | 0.00107 | 0.000 |
| I/O | 0.000 | 0.000 | 0.000 | 0.000 |
| Misc\_seq | 1.07 | 0.00022 | 1.07 | 0.000 |
| Decap | 0.00065 | 0.00065 | 0.000 | 0.000 |
| Total | 1.40 | 0.0216 | 1.31 | 0.0737 |

The total number of metal shapes added during the PGA process are tabulated in Table VIII.

After performing PGA, the total power consumption of the design reduced to 1.29 W. This is shown in Table IX.

1. VSS Metal Shapes Created

|  |  |
| --- | --- |
| **VSS shapes created during PGA** | **Number of metal shapes added** |
| metal3 (M3) | 379995 |
| metal4 (C4) | 215164 |
| metal5 (C5) | 105712 |
| metal6 (C6) | 189576 |
| metal7 (C7) | 494155 |
| metal8 (K1) | 55922 |
| via2 (V2) | 1254204 |
| via3 (J3) | 2797032 |
| via4 (A4) | 1571189 |
| via5 (A5) | 1570023 |
| via6 (A6) | 3758196 |
| via7 (CK) | 52635 |

1. Power Calculation After PGA

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cell\_type** | **Total Power(W)** | **Leakage**  **Power(W)** | **Internal**  **Power(W)** | **Switching**  **Power(W)** |
| Combinational | 0.1755 | 0.015 | 0.0913 | 0.069 |
| Latch and FF | 0.04927 | 0.00222 | 0.04616 | 0.000901 |
| Memory | 0.00464 | 0.00405 | 0.000588 | 0.000 |
| I/O | 0.000 | 0.000 | 0.000 | 0.00 |
| Misc\_seq | 1.0665 | 0.00022 | 1.0663 | 0.000007 |
| Decap | 0.000648 | 0.000648 | 0.000 | 0.0000 |
| Total | 1.2966 | 0.02224 | 1.2044 | 0.0699 |

The existing IR values for different designs including their cell count and worst IR voltage drop is shown in Table X [4]. The IR voltage drop values using double row optimization technique using the staples is shown in Table XI [7].

1. Existing IR Values

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Design** | **Cell Count** | **Reg Count** | **Before**  **(mV)** | **After**  **(mV)** | **% Reduction** | **Top 10 cells** | **Top 1K cells** | **All cells** | **Iavg (A)** |
| DES | 45787 | 8808 | 116 | 82 | 29.31% | 27.12% | 16.18% | 9.08% | 31.12% |
| Ethernet Mac | 33437 | 10545 | 89 | 58 | 34.83% | 32.14% | 19.41% | 10.62% | 26.11% |
| AES | 105116 | 1595 | 82 | 65 | 20.73% | 20.49% | 12.09% | 7.45% | 16.34% |
| B19 | 12384 | 1485 | 81 | 57 | 29.63% | 29.37% | 21.37% | 7.15% | 37.04% |

1. IR voltage dropValues After Using Double Row Optimization (Existing Technique)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **Staples** | **Staples** |  | **IR drop**  **(mV, Avg)** |  | **IR voltage drop**  **(mV, Avg)** |  |
| **Design** | **Util** | **Init** | **Final(del%)** | **Init** | **Final(del%)** | **Init** | **Final(del%)** | **Runtime (s)** |
| M0 | 60% | 29109 | 33423(+14.8%) | 29 | 28(-3.4%) | 76 | 66(-13.2%) | 2666 |
| AES | 60% | 31355 | 37813(+20.6%) | 23 | 23(0.0%) | 51 | 47(-5.6%) | 2542.5 |
| MPEG | 60% | 75781 | 80951(+6.8%) | 24 | 24(0.0%) | 64 | 60(-6.3%) | 3700 |
| JPEG | 60% | 217467 | 244333(+12.4) | 28 | 27(-3.6%) | 84 | 84(-4.5%) | 16679 |

# Conclusion and Future Scope

DDR memory blocks are having higher complexities while scaling down to lower technologies. The use of PGA technique helps in reducing the overall effort to optimize EM and IR voltage drop. Compared to previous works like double row optimization, the manpower has reduced and an improvement in the IR voltage drop, and EM percentages is seen. In this paper, static EMIR run was fired. GSR file is used for providing the voltages and other constraints. The proposed design has reduced the IR voltage drop values to less than 2% of the VDD value (0.99 V) and concerning EM variation could converge to around 83%. Typically, the value of the EM violations should be less than 100%. Hotspot reduction has been done by adding the metal strips. Thus, it can be concluded that by adding metal strips, and by providing a stronger PDN, we can mitigate the hotspots and therefore reduce the IR voltage drop and EM violations. The worst violated path in the static run before clearing violations is in the M1 metal layer has a value of 28.50 mV, and EM violating path is 192%. The total power consumption is found to be 4.11 W before clearing the static EMIR run violations. The worst violating path for the static run after clearing violations is in the M1 layer has a value of 5.60 mV. The total power consumption is measured to be 1.4 W for the static run after clearing violations and, EM violating path is put down to 83%. After using PGA, the total power consumption is reduced to 1.29 W. Therefore, there is an IR voltage drop of 28.5 mV before PGA and 5.6mV after PGA. From the existing methodology (double row optimization) we can see an IR voltage drop of 29 mV as the worst instance drop.

As part of future work, the leakage current effects can be analysed by adjusting the parameter file with critical timing paths and spacing information (design rule check file). This might yield better results of IR drop.

# Acknowledgment

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